REDUCTION CALCULATOR IN FPGA BASED SWITCHING HUB FOR HIGH PERFORMANCE CLUSTERS

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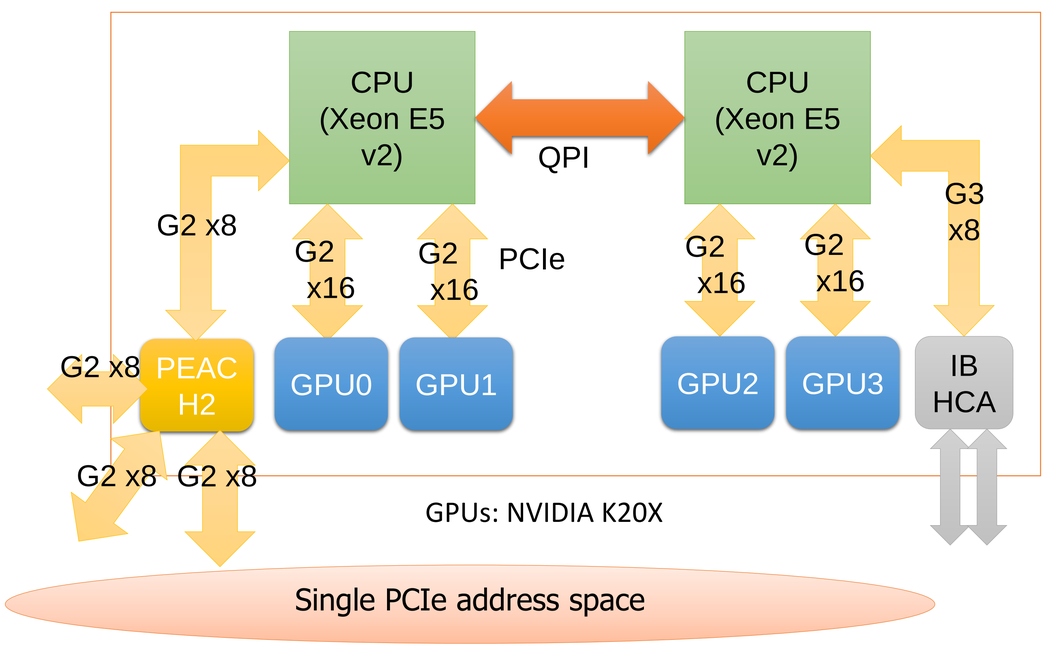
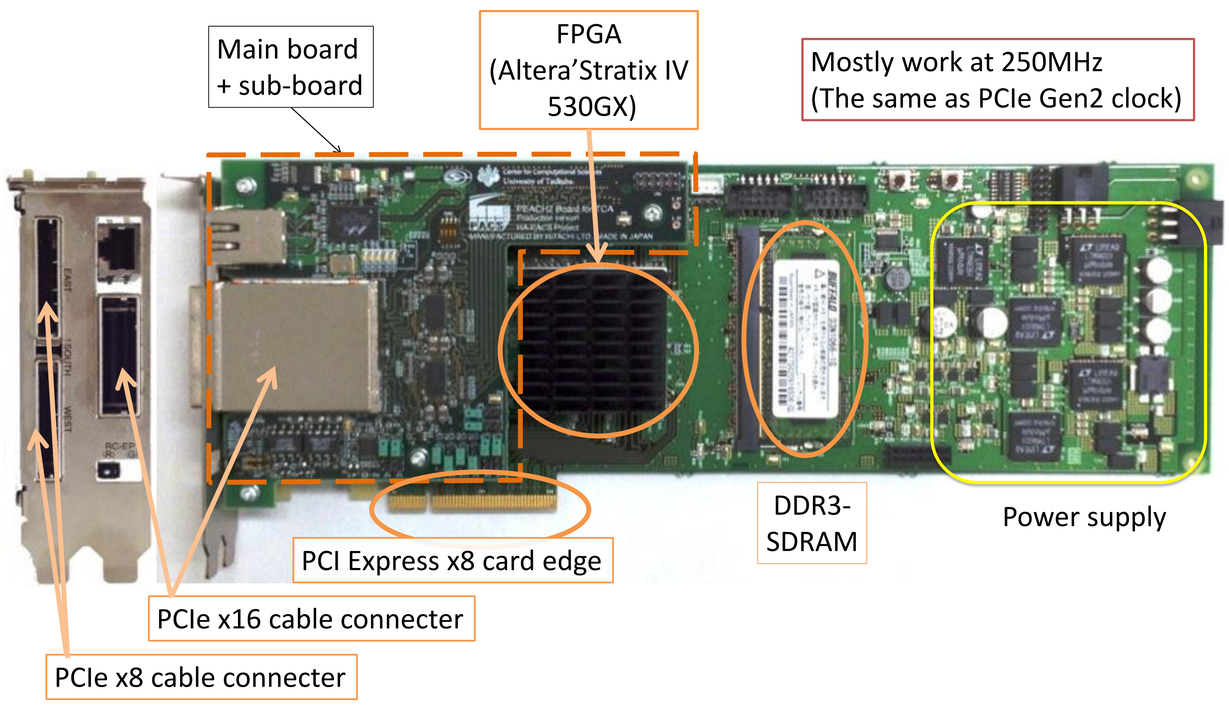
Computation in a Switching HUB

- FPGA is commonly used as a switching HUB in parallel systems.
- Unused logic in the FPGA can be used as an accelerator.
- Reduction calculator for solving radiative transfer equation is implemented on PEACH-2: a switching HUB for a supercomputer.

PEACH2: A low latency switching HUB



- Multiple Nodes with CPUs/GPUs can be directly connected with PEACH2 using PCIe Gen2 cables.
- All CPUs/GPUs are mapped on a single PCIe address space.
- Low latency (2.3µsec between GPUs) communication between GPUs is supported.
- 16 nodes can be connected at maximum with a double-ring network.



•PEACH2 board

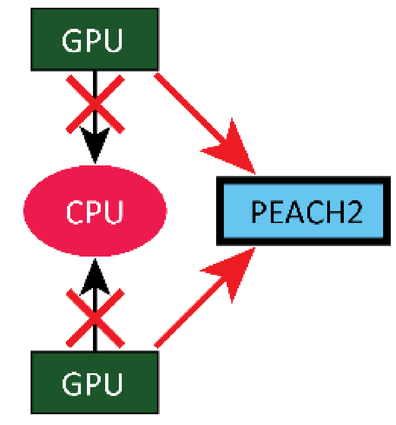
Target Application: ARGOT

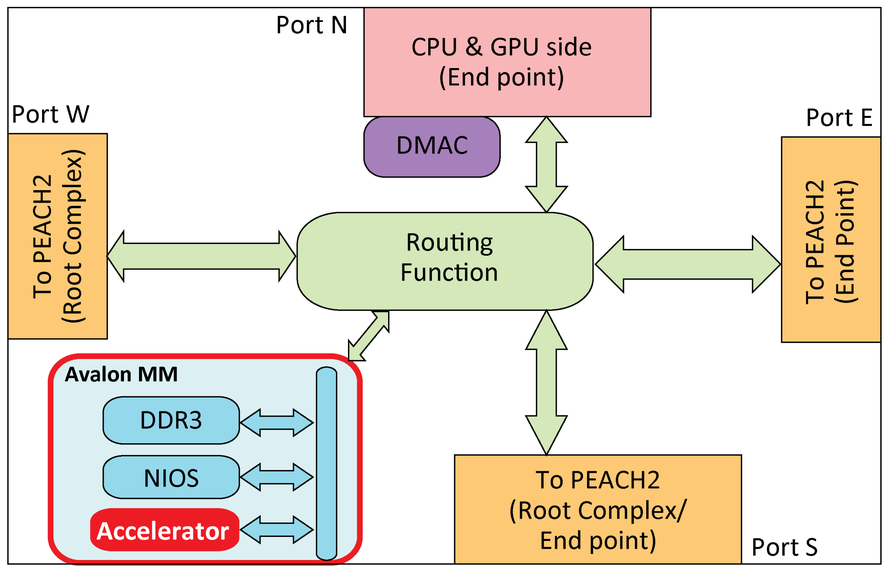
- Accelerated radiative transfer on grids using oct-tree.
- Solving the radiative transfer equation used for simulation of astronomical objects.
- Reduction calculation for eight particles must be frequently computed between GPUs.
- Since the computed results must be shared between GPUs, the reduction calculation is done in a CPU.

Reduction Calculator on PEACH2

•Multiple GPUs translate the data to PEACH2 and calculation is executed.

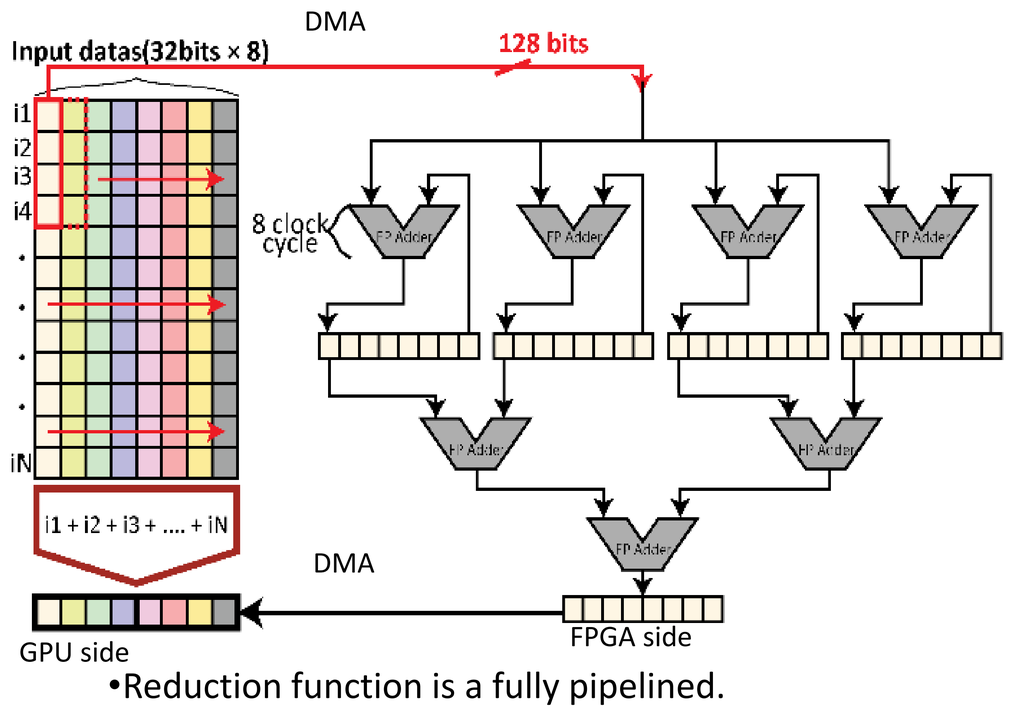
•GPU⇔CPU data communication is much reduced.





•Accelerator function is implemented with Avalon bus in PEACH2

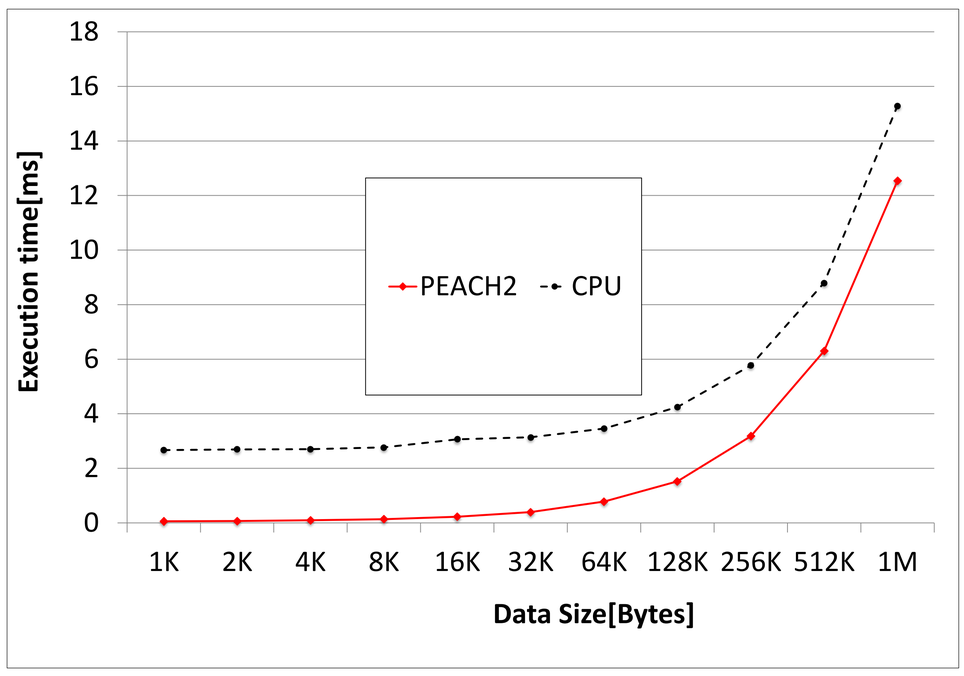
•Calculated data are translated from CPU/GPU using DMA



•Reduction function is a fully pipelined.

•Data input to the FPGA and write-back the result to GPU use DMA.

Evaluation/Summary



Execution time of reduction calculation of GPU data PEACH2 vs. CPU

•Resource utilization increases 1.3% in combinatorial logic and 1% in registers.

•Reduction logic works at 150MHz without disturbing switching hub facility.

•The performance is improved by 45 times at maximum.

•For large data size, the performance is degraded.