Faster and More Robust FPGAs

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Challenges to Scaling

Moore’s Law continues
- Transistors are still shrinking
- Stratix 10 at 5.5M LEs
- Density roadmap past 7nm

But there are challenges
- Dennard scaling ended ~2005
- Increasing variation of both delay, power
- Wafer cost rises with process complexity
Rising Development Cost and the FPGA Industry

Generally benefits FPGA, but that doesn’t make it fun

The good [FPGA incumbents]
- ASSP/ASIC starts still falling
- PLDs more attractive
- FPGA Si startup nearly impossible

The bad
- Lengthening TTM
- Fewer tape-outs per node

And the scary
- Process variation and design risk
- Design complexity (HW and SW)
2.5D Integration Helps

Multi-slice FPGA on Interposer

Stratix 10 SiP Transceiver Die
Increasing Hardened (ASIC) IP Helps

- Block Memory (9K/18K/20K) -> More block memory
- GPIO -> Hardened Memory Controllers
- Mult -> MAC -> DSP -> floating-point
- Processors -> +peripherals -> multi-core
- Transceivers -> +PCS -> +PCIe/Eth/ILKN
- Newer SOC devices: ++peripherals, RT, GPU, Codec
- Clearly coming: SIP memory and other ASIC

Hard IP is a clear win for the applications that use it. But also loads up the cost for the ones you don’t use.

**Smaller SOC FPGAs are less than 20% “FPGA”**
Insatiable I/O Bandwidth

Wireline will go 100G -> 400G -> Tb

Wireless data rates climbing for 4G and 5G

Optical FPGA Initiative
For the FPGA fabric, however…

Need to increase routing throughput
Stratix 10 Big Rocks

- 2X the achievable performance of Stratix V
- At up to 70% lower power

- Heterogeneous 3D System In Package (SiP) integration
- Adoption of Intel 14nm tri-Gate process

- Hierarchical configuration and security
- Modular design for verification
- Robustness – safety, security and SEU mitigation

- Expansion of new-market requirements
  - Multi-Core Processors, Floating-Point, Partial Reconfiguration
Acknowledgements

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Stratix 10 Innovations: All-in on 2.5D SiP

- Multi-Die via EMIB
  - Separate core / transceiver
  - Embedded Multi-Die Interconnect Bridge

FPGA Core Die

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Stratix 10 Innovations: Configuration & Clocking

- Multi-Die via EMIB
  - Separate core / transceiver
  - Embedded Multi-Die Interconnect Bridge

- Scalable Sector Architecture
  - Software Configuration
  - Configuration NoC
  - Routable Clocks
Stratix 10 Innovations: HyperFlex

- Multi-Die via EMIB
  - Separate core / transceiver
  - Embedded Multi-Die Interconnect Bridge

- Scalable Sector Architecture
  - Software Configuration
  - Configuration NoC
  - Routable Clocks

- Core Performance
  - HyperFlex Fabric, Tri-Gate
  - 1GHz M20K and DSP MAC
  - 750 MHz Floating Point
Stratix 10 Innovations: SoC & Memory

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  - Separate core / transceiver
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- 3rd Generation SoC
  - 1.5GHz ARM® Cortex A53
  - DDR I/O Banks with Hard Memory Controller
**Benefits**

- Reduced complexity vs. full interposer, and no reticle limit
- De-Couple analog (transceiver) development from digital FPGA fabric
- Transceiver reliability & yield enhancement
  - Don’t need rectangular “die”
  - Matching transceiver speed-grades
- Tick mixed with tock for added derivatives
  - E.g. 56G transceiver tile
  - E.g. new hardened I/O interface IP
  - E.g. SiP Memory or ASIC tiles
Processors for Infrastructure

Digitally-Assisted Analog

Transceiver and GPIO
- Hard microprocessors for calibration
- Used to manage process variation
- Also PMA/PCS reconfiguration

Expanded Role in Stratix 10
- Now for configuration and standalone infrastructure
FPGA Configuration Sub-System

CSS manages CRAM

Historically just a shift register
- AR/DR to Configuration RAM Array
- FSM controlled

Modern configuration adds significant system functionality
- Encryption, decryption, bitstream compression, redundancy
- Security: authentication, side-Channel, firewall, PUF
- SEU, scrubbing, partial re-configuration management
- Debug and Test

Our solution: move it to software
- More robust, upgradable, and risk-averse
Software-Defined Configuration

Secure Device Manager (SDM)
- Config and Re-Config, compression
- Security: authentication, encryption, PUF
- Maintenance (power, T/V, SEU, debug)

Local Sector Manager (LSM)
- Sector configuration manager

Config Network-on-Chip (CNoC)
- High-bandwidth SDM/LSM Communication
Sectors: Changing the World of Configuration

Partial Reconfiguration

SEU and Scrubbing

Security and Firewall
3rd Generation SoC Application Processor

1.5 GHz Quad-Core ARM® Cortex™ A53

- 28nm and 20nm used dual-core A9, 14nm moves to quad-A53
- CCU: Cache-coherency between FPGA accelerators and processors
- Integrated with configuration subsystem (SDM) – sharing peripherals
FPGA Fabric Building Blocks

Adaptive Logic Module

ALM Fracturing

Block RAM speed now 1GHz
New Data Coherency
New Quad-Port

LIM/LEIM/DIM fabric

H3/6 -> H2/4/10
V4 -> V3/4
10 TFLOPs Floating Point

- 1GHz fixed point MAC
- 750 MHz floating point +, *
- Already more power-efficient than GPU
- FPGA now winning in raw performance

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<table>
<thead>
<tr>
<th>Platform</th>
<th>Library/OS</th>
<th>ImageNet 1K Inference Throughput</th>
<th>Peak TFLOPs</th>
<th>Effective TFLOPs</th>
<th>Peak Power Required</th>
<th>Peak Power for CNN Compute (Projected)</th>
<th>Estimated GOPS/J (assuming peak power)</th>
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<td>16-core, 2-socket Xeon E5-2450, 2.1GHz</td>
<td>Caffe + Intel MKL Ubuntu 14.04.1*</td>
<td>53 images/s</td>
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<td>NervanaSys-32 on Ubuntu 14.04*</td>
<td>4129 images/s</td>
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<td>5.4T (82%)</td>
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</tbody>
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[Eric Chung (Microsoft), HotChips 2015]
Routable Clocking

- SW-routed clocks in sector “seams”
- More efficient use of globals
- Active skew management

(Legacy) Global Spines

Stratix 10 Routed Clocks
Fabric Performance and Power

Performance:
- A complete “re-think” on the philosophy of FPGA Fabric Architecture
- Registers are not just logic resources, they are routing resources
- Goal is to enable seamless movement and addition (pipelining) of registers
- Target: 2X the performance, without making the wires “2x faster”

Power:
- 14nm Tri-Gate process (FinFET) provides most of the benefit for power
- Expanded use of VID and power management adds more
  - High-Performance 800 mV to 940 mV
  - Low-Power options from 850 mV down to 800 mV
- HyperFlex for power reduction
  - Combine performance from HyperFlex with low-power options
- Target: 50% to 70% lower power per function, without slowing down
Re-timing and Pipelining in Conventional FPGAs

**Re-timing**
- Balance flops
- 16% \( f_{\text{max}} \) gain
- Added area

**Pipelining**
- Add flops
- 40% \( f_{\text{max}} \) gain
- Added clock tick
- Added area

**Raw Logic**
- Unbalanced paths
Routing muxes (all H/V wires) have *optional* registers
- Including LAB, M20K and DSP block inputs, CC, SCLR/CE

Architectural Goals:
- Perfect balance – P&R chooses the right register (of many) to turn on
- Simple Software – Re-timing is a simple push/pull along the path
- No wasted LEs – Designs with high FF:LUT ratios no longer an issue
- No wasted routing – Don’t have to route to find an available FF
Moving a Register in the HyperFlex fabric

- Disable in ALM, add to routing
- Moving a register is a push/pull operation on the route
- There is always a register on the routing mux
- Quartus® II chooses the most appropriate FF for path balancing
Re-timing and Pipelining in Stratix 10

Re-timing
- Balance flops
- 40% f_{max} gain
- Same resources

Pipelining
- Add flop
- Add clock tick
- 2X f_{max} gain
- Same resources

Raw Logic
- Unbalanced paths

Before Retiming
286MHz
- 1.5ns
- 3.5ns

Hyper Retiming
400MHz
- 2.5ns
- 2.5ns

Hyper Pipelining
572MHz
- 1.5ns
- 1.75ns
- 1.75ns

Hyper-Register

End to end latency: (3 ticks, 5ns) -> (4 ticks, 5ns)

Throughput: 2X packets/sec
Software for HyperFlex

Software adds a new re-timing step, post-route

Re-Timing is a simplified operation, easily verified

HyperFlex
Primitive
A New Perspective on Timing Closure

- SP&R Anticipates Retiming
  - Critical domains/chains
  - Not volatile register-register paths

- And is not afraid to ask for help:

```
Recommended Registers to Insert into Clock Domain set_host_clk

1  Need up to 2 registers on 32 paths from set_clk to set_host_clk
   insert at least 2 registers
   From ups_reg_file:reg_file|dout[6]
   To ups_reg_file:reg_file|dout_q0[6]
   insert at least 2 registers
   From ups_reg_file:reg_file|dout[7]

Recommended Registers to Modify in Clock Domain set_host_clk

1  Remove user preserve assignments from 91 registers in Clock Domain set_h
   Remove user preserve assignments from ups_reg_file:reg_file|host_ack
```
Optimizing Designs with HyperFlex

Hyper-Pipeline the Datapath

Latency Tolerance
(ticks, not total)

Optimize Control Logic
High-Level Languages and HyperFlex

- OpenCL, C (HLS), DSP Builder are inherently un-timed
  - Tool chooses pipelining strategy, not specified in RTL

- Streaming (throughput) based dataflow is latency insensitive

- These applications get high-performance at low effort

- Example: Most DSP filters generated by DSP Builder naturally come out at 1GHz operation.
Datapath Width – Routability and Power

100Gb Ethernet in Arria 10: 390 MHz at 320b

Next generation?
- Without help, 200Gb requires 640b, 400Gb requires 1280b
- Fabric wire-count cannot double – at best sqrt(2) * 1.15
- But HyperFlex gets us to 781 MHz, using the wires more efficiently

Running at half datapath-width
- Half the width means half the area
- Which means half the static power on the same device.

DSP at 2X folding rate
- With HyperFlex to support pipelining, limited only by 1GHz DSP/M20K
Area/Delay/Power Tradeoffs with Stratix 10

Stratix V Migrate to
Stratix 10

½ Width
2x f_{max}

2X
Throughput

I/O
AC
DC

HyperFlex™

3X
Power

HyperFlex™

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Looking Forward - Old Markets and New

- SDN and 5G are all-programmable
  - A huge opportunity for FPGAs in our traditional markets as router flexibility requirements grow and cannot be served by fixed-ASIC

- FPGAs will *explode* into datacenter and virtualization
  - Smarter NIC/switch, attached acceleration, FPGA in the cloud
  - CNN for search and vision accelerations [Microsoft, others]
  - These are the new markets for high-end FPGAs

- But there are still problems to solve:
  - Compilation for over 10M LEs required for 10nm
  - C-gates efficiency has to get way better for Comms to use it
  - TriGate was a big catch-up on power. We need more.
Summary

- 3D integration isn’t just integration, it is
  - De-risking, process matching, derivative proliferation and tick/tock

- Device floorplanning and configuration makeover
  - Software control allows for security and feature-up of devices

- SoC integration is mainstream
  - Processor cost is a small subset of the die, coherent-accelerators

- Pipelining unlocks optimizations in FPGA architecture
  - Using wires efficiently, not brute-forcing them faster
  - Faster == lower power when you can get designs to a more efficient place

- Process is still giving us power benefits
  - 14nm Tri-Gate reduces power, enabling higher performance circuit-design
Thank You