Design and Simulation Tools for **Embedded NoCs**

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FPGA NoC DESIGNER

«Compare area/freq./power of hard and soft NoCs»

www.eecg.utoronto.ca/~mohamed/noc_designer

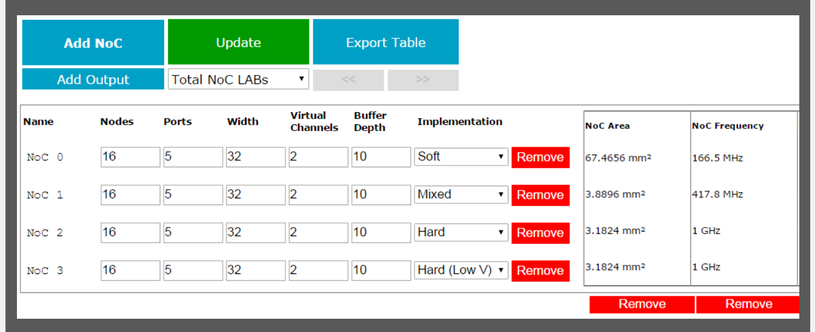
WHY? To motivate hardening NoCs (or NoC components) in FPGAs, the first step was to measure the efficiency of the NoC sub-components when implemented hard using ASIC technology, or soft in the FPGA fabric.

WHAT? We implemented a packet-switched virtual-channel router using Synopsys design compiler and Altera Quartus II tools, and gathered accurate area, frequency and power measurements for NoCs of different parameters. On average, hard NoCs are 23x smaller, 6x faster and 11x lower power.

HOW? NoC Designer uses the database of measurements to compute and plot efficiency metrics for *any* NoC parameters. If the requested NoC is not in the database of measured data, NoC designer interpolates between the measured points to compute an estimate.

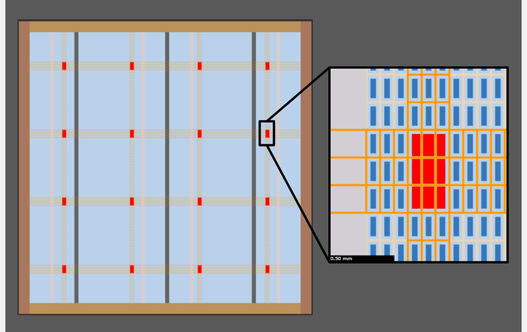
SCREENSHOTS

System-level Table View



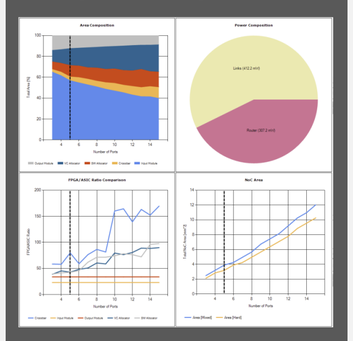
The user can add soft, mixed or hard NoCs in the table and configure their parameters. The tool calculates various system-level metrics such as area, frequency, or compound parameters such as energy per data.

Visualization View



The user can zoom in to see the size of routers and logic blocks to scale, and click to know more information about NoC elements.

Graph Analysis View



Detailed analysis of NoC subcomponents using graphs to view trends.

RTL2BOOKSIM

«Connect RTL designs to a flexible NoC simulator»

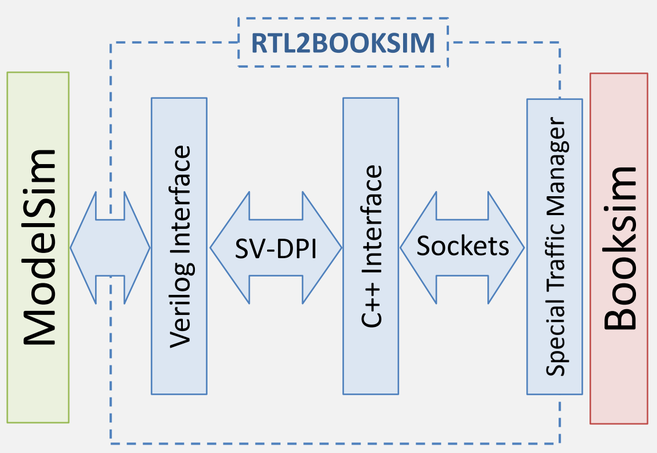
www.eecg.utoronto.ca/~mohamed/rtl2booksim

WHY? We needed to show that embedded NoCs can *actually* be used to interconnect important FPGA applications. It is also necessary to be able to measure the cycle-accurate behaviour of these applications to quantify performance (latency and throughput).

WHAT? Booksim is a widely-used, flexible, cycle-accurate, C++ simulator. We want to use Booksim to model our embedded NoC in complex FPGA designs written in RTL (Verilog or VHDL).

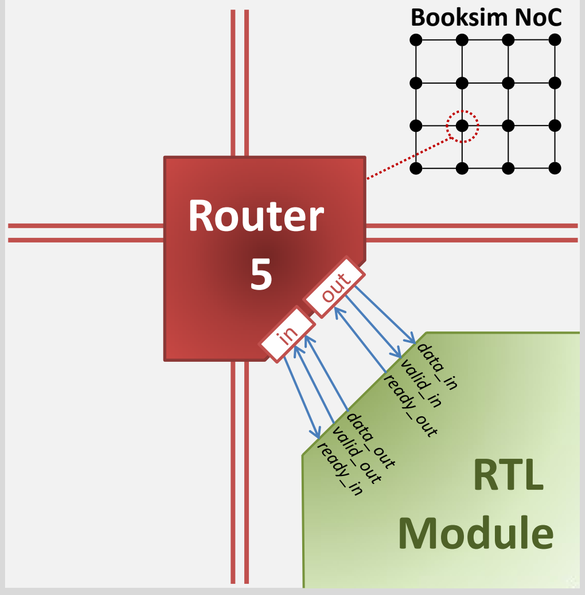
HOW? We modified Booksim so that it can communicate with other programs by adding a socket interface. We then created bindings to Booksim using SystemVerilog DPI (SV-DPI) which allowed us to connect RTL (Verilog) modules to NoC routers in Booksim, and simulate the whole system in Mentor ModelSim.

BLOCK DIAGRAM



To use Booksim within an RTL simulation (e.g. in Modelsim) , we created bindings using socket programming and SystemVerilog DPI. The block diagram shows the basics of how RTL2Booksim works.

NOC CONNECTIVITY



VERILOG INSTANTIATION

```
noc_wrapper #(
  .WIDTH_NOC   (150),
  .N           (16),
  .NUM_VC      (2),
  .DEPTH_PER_VC (16),
  .VERBOSE     (0)
)
noc_inst (
  .clk_noc (…),
  .clk_rtl (…),
  .rst     (…),

  .r5_data_in  (…),
  .r5_valid_in (…),
  .r5_ready_out(…),

  .r5_data_out (…),
  .r5_valid_out(…),
  .r5_ready_in (…),
   ...
);
```

NoC Parameters

Clocking and reset

Router #5 ports

To use RTL2ooksim, instantiate and connect an “noc_wrapper” module in your design.

LYNX CAD FOR FPGA NOCS

«Automatically connect FPGA applications with NoCs»

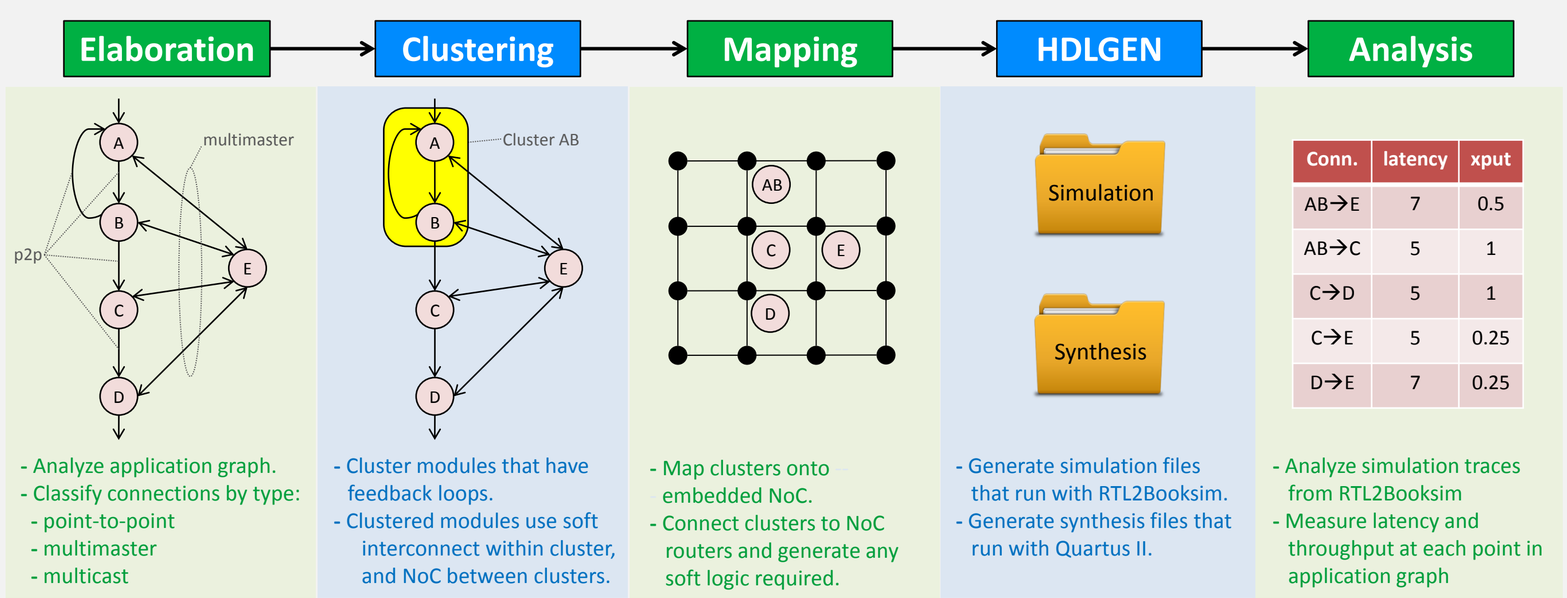
www.eecg.utoronto.ca/~mohamed/lynx

WHY? Efficiently using an embedded NoC requires *some* advanced knowledge about how NoCs work. However, a computer-aided design (CAD) tool can be created to automatically connect a user application to an embedded NoC and leverage all of its features for the application.

WHAT? LYNX is a CAD framework for entering an application connectivity graph, and interconnecting the application modules using a form of system-level interconnect. The CAD tool is general enough to work with any interconnect type, but we use it primarily for embedded NoCs.

HOW? LYNX takes an XML description of an application’s connectivity graph and maps that onto an NoC, and instantiates any soft logic required. Both synthesis and simulation files are generated which the user can run in vendor tools like Altera Quartus II or Mentor ModelSim.

CAD FLOW



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ALTERA

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