Dynamic Voltage and Frequency Scaling: a Real-world Example

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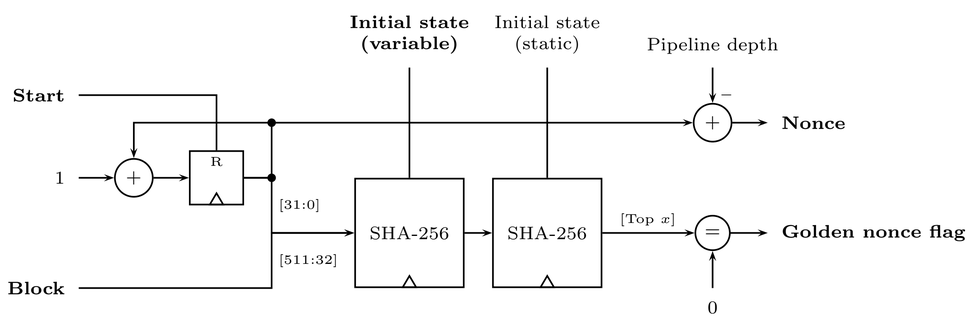
PRiME Project

- Stands for **P**ower-efficient, **R**eli**i**able **M**any-core **E**mbedded systems
- £5.6-million ($8.6-million) UK government-funded research programme
- Involves Imperial College London and the Universities of Southampton, Newcastle and Manchester
- Four main 'themes'
  1. Cross-layer theory and models
  2. Runtime management and optimisation
  3. Many-core architectures and reconfiguration
  4. Platforms, applications and demonstrators

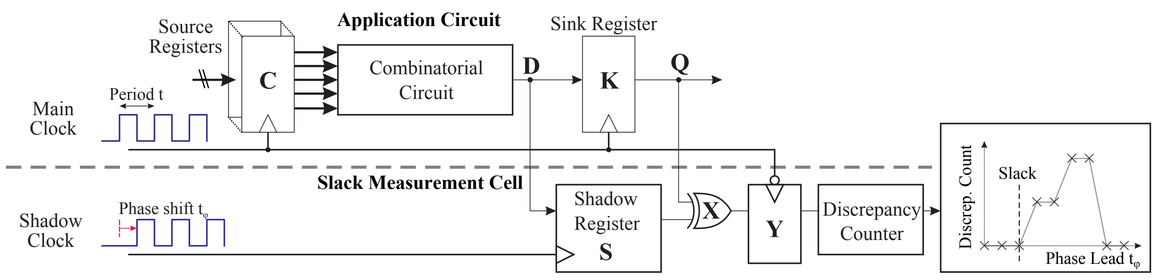
Application

- Chosen application: Bitcoin mining
- **Bitcoin** is a decentralised, cryptographic currency
- **Mining** is the process of creating new money: hard to do, easy to verify
- Core computation is performed by two chained SHA-256 hashers, accelerated in hardware on an FPGA
- Goal: find a nonce that, when hashed with a data block, produces an output with x leading zeroes
- Hash rate $\implies$ rate of monetary return

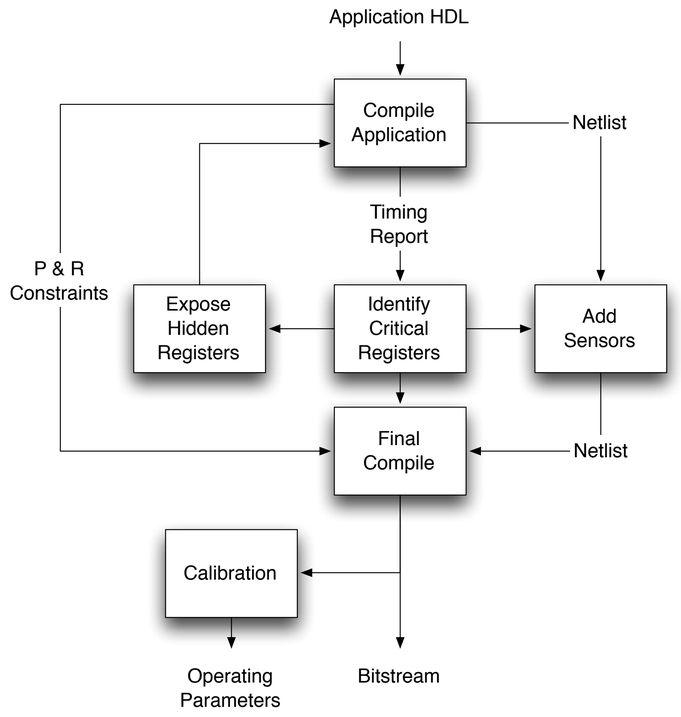


Slack Measurement

- Operating margins, in the form of **timing slack**, are added to designs to counter effects including
  - → Supply voltage fluctuation
  - → Temperature change
  - → Process variation
  - → Degradation
- These tend to be very conservative, and become greater as process geometry decreases
  - → Greater performance and/or energy efficiency possible
- By collecting information from a circuit as it is running, these margins can be safely eroded
- Slack within a particular path is measured by
  - → Replicating, or **shadowing**, that path's sink register
  - → Feeding the shadowed register with a shifted (leading) clock of variable phase
  - → Phase shift required to cause discrepancy $\implies$ slack

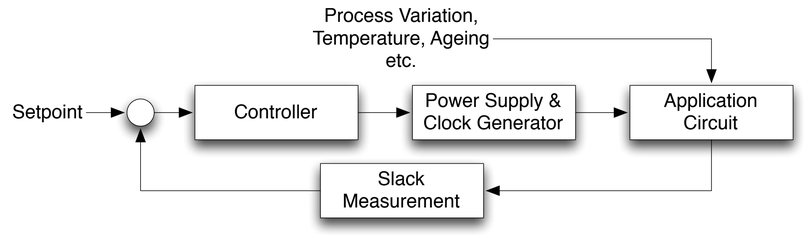


- CAD flow developed to
  - → Synthesise, pack, place and route application circuit as normal
  - → Identify **critical** paths most likely to experience timing failure
  - → Insert, post-place and route, slack monitoring logic using spare resources
- Before use, calibration must be performed to counter path length differences and clock skew

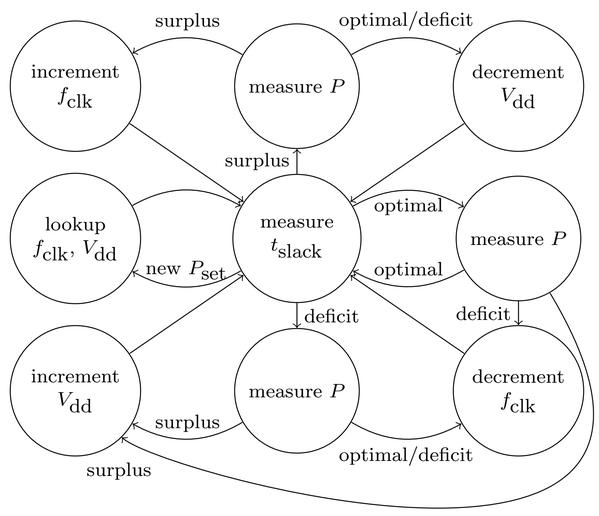


Dynamic Scaling

- Hasher and control logic placed in separate, variable-frequency clock domain
- Design instrumented with slack measurement logic
- Voltage and frequency scaled dependent upon operating requirements and available slack
  - → Voltage: variable external power supply
  - → Frequency: dynamically reconfigurable on-die PLL

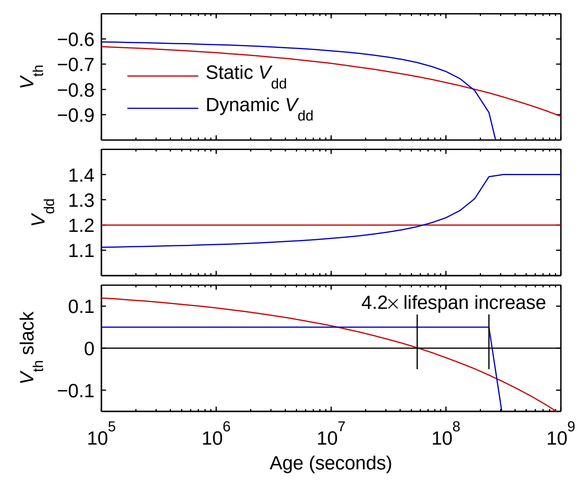


- Control loop can be set to meet constraints on
  - → Frequency (minimise voltage $\implies$ minimum power)
  - → Voltage (maximise frequency $\implies$ maximum performance)
  - → Power (optimise for both voltage and frequency)



Advantages

- Higher performance for same power or lower power for same performance
- Automatic adaptation to physical and environmental changes over time
- Allowing V_{dd} to track degradation-induced changes in V_{th} allows lifespan to be increased



Further Reading

- PRiME Project
  - → http://www.prime-project.org/
- Bitcoin
  - → S. Nakamoto, "Bitcoin: A Peer-to-Peer Electronic Cash System," *Consulted*, vol. 1, no. 2012, 2008.
  - → http://en.bitcoin.it/wiki/Block_hashing_algorithm
- Slack measurement and dynamic voltage & frequency scaling
  - → J. M. Levine, E. Stott, G. A. Constantinides, and P. Y. K. Cheung, "Online Measurement of Timing in Circuits: For Health Monitoring and Dynamic Voltage & Frequency Scaling," *International Symposium on Field-programmable Custom Computing Machines (FCCM)*, 2012.
  - → J. M. Levine, E. Stott, G. A. Constantinides, and P. Y. K. Cheung, "SMI: Slack Measurement Insertion for online timing monitoring in FPGAs," *International Conference on Field Programmable Logic and Applications (FPL)*, 2013.
  - → E. Stott, J. M. Levine, P. Y. K. Cheung, and N. Kapre, "Timing Fault Detection in FPGA-based Circuits," *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2014.
- Reliability of FPGA-implemented logic
  - → E. Stott, P. Sedcole, and P. Y. K. Cheung, "Fault Tolerance and Reliability in Field-programmable Gate Arrays," *IET Computers and Digital Techniques*, vol. 4, no. 3, 2010.
  - → E. Stott, Z. Guan, J. M. Levine, J. S. J. Wong, and P. Y. K. Cheung, "Variation and Reliability in FPGAs," *IEEE Design & Test*, vol. 30, no. 6, 2013.